AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

Claim 1 (Currently Amended) An image array having a plurality of pixels disposed in rows and columns, wherein each pixel includes a photodiode, a thin film transistor (TFT), and a clamping diode, the image array further comprising:

a plurality of data lines, each of the plurality of data lines coupled to each of a source or a drain of the thin film transistor of row or a column of pixels;

a plurality of gate lines, each of the plurality of gate lines coupled to each of a gate of the thin film transistor of a column or a row of pixels;

a plurality of bias lines carrying a bias voltage, each of the plurality of bias lines coupled to each of an anode of the photodiode of the pixels in a row or a column of pixels; and

a plurality of clamp lines electrically interconnecting the clamping diodes in individual ones of the rows or columns of the array, wherein the clamp lines carry a clamping voltage.

Claim 2 (Original) The image array of claim 1, wherein the clamping diode in each pixel is electrically connected between a storage node of the photodiode and the clamp line.

Claim 3 (Original) The image array of claim 1, wherein the clamping voltage keeps the photodiode under reverse bias.

Claim 4 (Original) The image array of claim 3, wherein the clamping voltage is between about -4 to -5 V with respect to the potential of the data line.

Claim 5 (Original) The image array of claim 1, wherein the clamping diode has a forward bias when the photodiode becomes overexposed.

Claim 6 (Original) The image array of claim 5, wherein the clamping diode has a forward bias of about 0.1 V at the initial stages of overexposure.

Claim 7 (Original) The image array of claim 1, wherein the bias voltage is about -8 to -10 volts.

Claim 8 (currently amended) A clamping circuit in a sensor array that reduces lag comprising:

a gate line;

a data line;

a bias line carrying a bias voltage ~~$V_{bias;}$~~ $V_{bias;}$

a clamp line carrying a clamping voltage V_{clamp};

a TFT having a source, a drain, and a gate, wherein the source or drain of the TFT is connected to the data line and the gate is connected to the gate line;

a photodiode having an anode, ~~a cathode,~~ and a storage node, wherein the ~~anode~~ storage node is connected to the other of the source or drain of the TFT and the ~~cathode~~ anode is connected to the bias line; and

a clamp diode having an anode and cathode, wherein the clamp diode anode is connected to the clamp line and the clamp diode cathode is connected to the storage node of the photodiode.

Claims 9-18 (Cancelled).